UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/517,818	12/14/2004	Suk Hun Lee	3449-0413PUS1	8713

2292 7590 12/26/2008

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
INGHAM, JOHN C	

ART UNIT	PAPER NUMBER
2814	

NOTIFICATION DATE	DELIVERY MODE
12/26/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No. 10/517,818	Applicant(s) LEE, SUK HUN	
	Examiner JOHN C. INGHAM	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21,23-29,31,33-36 and 38-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21,23-29,31,33-36 and 38-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 18 September 2008 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims **21, 23, 31, 33-35, 36, 38 and 40** are rejected under 35 U.S.C. 103(a) as being unpatentable over Takashi, Kaneyama and Koide.

4. Regarding claims **21 and 31**, Takashi discloses in the abstract figure a nitride semiconductor LED, comprising: a substrate (1); a buffer layer (2, 3 and first layers of item 30) formed on the substrate, wherein the buffer layer has a triple-structured III-V nitride semiconductor film laminated (¶51-56); an undoped GaN layer (4) on the buffer layer; AlGaN/GaN short period superlattice layers (40 and 50, may be AlGaN/GaN as described in ¶11) formed on the undoped GaN layer (4) in a sandwich structure of

upper and lower layers having an undoped GaN layer (5) interposed therebetween; a first electrode layer of an n+ GaN layer (6, 7 contact layers are highly doped for conductivity) formed above and in direct contact with the upper SPS layer; an n type GaN based layer (9, clad layer) formed on the first electrode layer and containing a low concentration of dopants (clad layers doped lower for bandgap); an active layer (11) formed on the n type GaN based layer; and a second electrode layer (15) of p-GaN layer formed on the active layer.

5. Takashi does not specify wherein the buffer layer (2, 3 and 30) has a triple-structured $Al_yIn_xGa_{(1-x-y)}N/In_xGa_{1-x}N/GaN$ laminated where $0<x\leq1$, $0\leq y\leq1$. Instead Takashi discloses that the triple layer structure is AlGaN/GaN/InGaN. However, Kaneyama teaches that it is well known that III-V nitride materials used for buffer layers follow the general formula: $Al_xIn_yGa_{(1-x-y)}N$, which includes the quaternary, ternary, and binary alloys of Al, In, Ga, and N (col 2 ln 20-26). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Kaneyama on the device of Takashi since a buffer layer comprising a quaternary III-V material formed of Al, In, Ga, and N (AlInGaN) is a suitable alternative for the AlGaN layer as disclosed by Takashi. One of ordinary skill in the art would have been motivated to look to analogous art teaching alternative buffer materials, and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

6. Takashi also does not specify wherein the n type GaN based layer (9) is a current leakage prevention layer. Koide teaches that the dopant concentration of the n-GaN clad layer is approximately $1x10^{17}/cm^3$ (¶48). It would have been obvious to one of

ordinary skill in the art at the time of the invention to use these values since these values are well known in the art. The low dopant concentration is known and improves the band gap of the n- GaN clad layer (e.g. Hatano col 8 ln 20 describes dopant relationship to resistance in LEDs). The dopant concentration of the clad layer has lower conductivity and will therefore function as a current leakage prevention layer.

7. Regarding claim **23**, Takashi discloses the LED of claim 21, further comprising an undoped GaN layer (4) on the GaN based buffer layer (2, 3 and 30), wherein the first GaN based layer (6) is n type and the second GaN based layer (15) is p type.

8. Regarding claims **35-36 and 38**, Takashi discloses a fabrication method of a nitride semiconductor LED, comprising: forming a buffer layer (¶51, item 2, 3 and 30) on a substrate; forming an undoped GaN layer (4) on the buffer layer; forming $Al_yGa_{1-y}N$/ GaN short period superlattice layers (40, 50) on the buffer layer in a sandwich structure of upper and lower layers having an undoped GaN layer (5) interposed therebetween (¶54); forming a first n type GaN based layer (6, 7) above and in direct contact with the upper SPS layer; forming an n type GaN based layer (9) containing a low concentration of dopants between the first GaN based layer of a n+ GaN layer (7) and the active layer; forming an active layer (¶84, item 11) on the first GaN based layer; and forming a second GaN based layer (15) of a p-GaN layer on the active layer (¶86).

9. Takashi does not specify wherein the buffer layer (2, 3 and 30) has a triple-structured $Al_yIn_xGa_{(1-x-y)}N/In_xGa_{1-x}N/GaN$ laminated where $0<x\leq1$, $0\leq y\leq1$. Instead Takashi discloses that the triple layer structure is AlGaN/GaN/InGaN. However, Kaneyama teaches that it is well known that materials used for buffer layers follow the

general formula: $Al_xIn_yGa_{(1-x-y)}N$, which includes the quaternary, ternary, and binary alloys of Al, In, Ga, and N (ALInGaN, col 2 ln 20-26). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Kaneyama on the device of Takashi since a buffer layer of AlInGaN a suitable alternative for the AlGaN layer as disclosed by Takashi. One of ordinary skill in the art would have been motivated to look to analogous art teaching alternative buffer materials, and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

10. Takashi also does not specify wherein the n type GaN based layer (9) is a current leakage prevention layer. Koide teaches that the dopant concentration of the n-GaN clad layer is approximately $1x10^{17}/cm^3$ (¶48). It would have been obvious to one of ordinary skill in the art at the time of the invention to use these values since these values are well known in the art. The low dopant concentration is known and improves the band gap of the n- GaN clad layer (e.g. Hatano col 8 ln 20 describes dopant relationship to resistance in LEDs). The dopant concentration of the clad layer has lower conductivity and will therefore function as a current leakage prevention layer.

11. Regarding claims **33, 34 and 40**, Koide teaches that the dopant concentration of the n+ GaN contact layer in an LED is more than $1x10^{18}/cm^3$ (¶48) and the dopant concentration of the n-GaN clad layer is approximately $1x10^{17}/cm^3$ (¶48).

12. Claims **24-29** are rejected under 35 U.S.C. 103(a) as being unpatentable over Takashi, Koike and Koide.

13. Regarding claims **24 and 27**, Takashi discloses in the abstract figure a nitride semiconductor LED, comprising: a substrate (1); a buffer layer (2, 3 and 30) formed on the substrate; an undoped GaN layer (4) on the buffer layer; AlGaN/GaN short period superlattice layers (40 and 50, may be AlGaN/GaN as described in ¶11) formed on the undoped GaN layer (4) in a sandwich structure of upper and lower layers having an undoped GaN layer (5) interposed therebetween; a first GaN based layer (6 and 7) above the upper SPS layer (50); an n type GaN based layer (9) of the first GaN based layer; an active layer (11) formed on the n type GaN based layer; and a second GaN based layer (15) of p-GaN formed on the active layer. GaN layers (6 and 7) are considered integral because they are of the same material (layer 7 is grown on layer 6 so even the lattice constants match) and of the same conductivity (layer 6 is undoped GaN, which is generally UID n-type, see Edmond US 6,800,876 col 7 ln 24).

14. Takashi does not specify that the GaN layer on the buffer layer is indium-doped, or that short period superlattice includes an indium-doped GaN layer interposed between the AlGaN/GaN layers. Instead Takashi uses undoped GaN layers. However, Koike teaches that when GaN is doped with indium, the layer will exhibit significantly good crystallinity and compensate for strains due to defects (col 22 ln 60 - col 23 ln 5). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Koike on the device of Takashi in order to reduce defects and produce a layer with good crystallinity.

15. Takashi also does not specify wherein the first n type GaN based layer (6) contains a high concentration of dopants and the n type GaN based layer (9) is a current leakage prevention layer. Koide teaches that the dopant concentration of the n+ GaN contact layer in an LED is more than $1x10^{18}/cm^3$ (¶48) and the dopant concentration of the n-GaN clad layer is approximately $1x10^{17}/cm^3$ (¶48).It would have been obvious to one of ordinary skill in the art at the time of the invention to use these values since these values are well known in the art. The low dopant concentration is known and improves the band gap of the n- GaN clad layer (e.g. Hatano col 8 ln 20 describes dopant relationship to resistance in LEDs). The dopant concentration of the clad layer has lower conductivity and will therefore function as a current leakage prevention layer.

16. Regarding claim **25 and 28,** Takashi discloses the LED of claims 24 and 27, wherein the GaN buffer layer (2, 3 and 30) has a triple-structured AlGaN/InGaN/GaN laminated (¶52).

17. Regarding claim **26**, Takashi discloses the LED of claim 24, further comprising the undoped GaN layer (4), or the indium-doped layer (layer 4 doped as taught by Koike) on the GaN based buffer layer (2, 3 and 30).

18. Regarding claims **29**, Koide teaches that the dopant concentration of the n+ GaN contact layer in an LED is more than $1x10^{18}/cm^3$ (¶48) and the dopant concentration of the n-GaN clad layer is approximately $1x10^{17}/cm^3$ (¶48).

19. Claim **39** is rejected under 35 U.S.C. 103(a) as being unpatentable over Takashi, Kaneyama and Koide, and further in view of Yuasa. Takashi, Kaneyama and Koide discloses the method of claim 35, wherein the layers are grown to a 50-400Å thickness (Takashi ¶34) at 800°C (¶70), but does not specify that the GaN buffer layer is formed using MOCVD equipment in an atmosphere having H_2 and N_2 carrier gases supplied while having TMGa, TMIn, TMAl source gas introduced and simultaneously having NH_3 gas introduced.

20. Yuasa teaches the formation of nitride films using MOCVD equipment at a growth temperature of 800°C (col 13 ln 66) in an atmosphere of H_2 and N_2 carrier gases supplied while TMGa and NH_3 are introduced simultaneously (col 13 ln 33). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Yuasa since the teachings produce a nitride film with good growth efficiency relative to the material supply amount (col 10 ln 20-23).

Response to Arguments

21. Applicant's arguments with respect to claims 21, 23-29, 31, 33-36 and 38-40 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN C. INGHAM whose telephone number is (571)272-8793. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Howard Weiss/
Primary Examiner
Art Unit 2814

John C Ingham
Examiner
Art Unit 2814

/J. C. I./
Examiner, Art Unit 2814